What is claimed is:

1. A mounting substrate, comprising:

a substrate body having at least first and second adjacent chip mounting regions defined on a surface thereof, and further having a dicing line defined between the first and second mounting regions;

a first plurality of inner electrodes aligned along a first side of the first chip mounting region;

a second plurality of inner electrodes aligned along a second side of the second chip mounting region, wherein the first side of the first chip mounting region confronts the second side of the second chip mounting region; and

an interconnect wiring pattern located between the first and second chip mounting region, and commonly connected to the first plurality of inner electrodes and the second plurality of inner electrodes, wherein the interconnect wiring pattern includes a plurality of connected wiring portions , and wherein at least some of said wiring pattern extend obliquely across the dicing line.

2. The mounting substrate according to claim 1, and wherein oher wiring patterns of the interconnect wiring pattern extend at right angle across the dicing line.

3. The mounting substrate according to claim 1, wherein the interconnecting wiring pattern has a zigzag configuration.

4. A method for manufacturing a semiconductor device, comprising:

providing a substrate body having at least first and second adjacent chip

mounting regions defined on a surface thereof, and further having a dicing line defined between the first and second mounting regions;

forming a first plurality of inner electrodes aligned along a first side of the first chip mounting region;

forming a second plurality of inner electrodes aligned along a second side of the second chip mounting region, wherein the first side of the first chip mounting region confronts the second side of the second chip mounting region;

forming an interconnect wiring pattern located between the first and second chip mounting region, and commonly connected to the first plurality of inner electrodes and the second plurality of inner electrodes, wherein the interconnect wiring pattern includes a plurality of connected wiring portions , and wherein at least some of said wiring pattern extend obliquely across the dicing line.

5. The method for manufacturing a semiconductor device according to claim 4, further comprising:

mounting a first and second semiconductor chips over the first and second mounting regions respectively;

electrically connecting a pad of the first semiconductor chip to the first plurality of inner electrodes;

electrically connecting a pad of the second semiconductor chip to the second plurality of inner electrodes; and

molding a resin over the first and second semiconductor chip;

dicing the mounting substrate along to the dicing line.